IN THE SPECIFICATION:

Please amend paragraph [0011] and [0047] of the specification as follows:

[0011] Similarly, as shown in one configuration of a semiconductor die stack assembly 600 known to the inventor herein (FIG. 6), a top semiconductor die 640 is stacked above a smaller bottom semiconductor die 620 in an active surface 622 of bottom semiconductor die 620 to backside 674 of top semiconductor die 640 arrangement. An optional adhesive layer 626, is shown between bottom semiconductor die 620 and top semiconductor die 640. Peripheral edges 664, 666 of the larger top semiconductor die 640 extend laterally beyond peripheral edges 660, 662 of the bottom semiconductor die 620. Similarly, a stacked board-on-chip assembly 700 is shown in FIG. 7 wherein a top semiconductor die 740 is stacked above a smaller, bottom semiconductor die 720 in a backside 724 of bottom semiconductor die 720 to backside 746 of top semiconductor die 740 arrangement. The peripheral edges 764, 766 of the larger top semiconductor die 740 extend laterally beyond the peripheral edges 760, 762 of the smaller bottom semiconductor die 720. A plurality of external solder balls 772 may be used for electrical connection of the encapsulated stacked board-on-chip assembly 700 to another assembly. FIG. 8 illustrates a configuration of a stacked semiconductor die assembly 800 known to the inventor herein depicting multiple devices on a substrate wherein each device includes two semiconductor dice in a laterally staggered arrangement. The die are stacked such that the active surface 822 of the bottom semiconductor die 820 faces the backside 846 of the top semiconductor die 840. [One] At least one peripheral edge 866, 864 of a top semiconductor die 840 extends laterally beyond a corresponding peripheral edge 862, 860 of a bottom semiconductor die 820. In FIGs. 6, 7 and 8, the top semiconductor dice 640, 740, 840 and the bottom semiconductor dice 620, 720, 820 are electrically connected to a substrate 630, 730, 830 via bond wires 628, 728, 828 that protrude above the uppermost semiconductor dice thereof (or as in FIG. 7, below the lower most semiconductor dice), thus necessitating a higher package height 648, 748, 848.

[0047] The stacked semiconductor package 900''' of FIG. 14 is similar to the stacked semiconductor package 900 depicted in FIG. 9. The backside 924''' of bottom semiconductor die 920''' may be disposed on a substrate 930'''. Alternatively, a one or more semiconductor die may be disposed between the bottom semiconductor die 920''' and the substrate 930'''. The bottom semiconductor die 920''' may be electrically connected to the substrate 930''' by way of discrete conductive elements 928'''. An insulative layer 926''' may be disposed between bottom semiconductor die 920''' and top semiconductor die 940'''. At least one peripheral edge 966''' of the top semiconductor die 940''' extends beyond a corresponding peripheral edge 962''' of the bottom semiconductor die 920''', and at least one peripheral edge 960''' of the bottom semiconductor die 920''' extends beyond a corresponding peripheral edge 964''' of the top semiconductor die 940'''. A first electrical connector 944''', such as a pillar column, bump, or ball of conductive material (e.g., solder, other metal, conductive or conductor filled epoxy, anistropically conductive elastomer, etc.), extends from a bond pad 942''' on the active surface 946''' of the top semiconductor die 940''' to its corresponding bond pad 936''' on the bottom semiconductor die 920'''. The active surface 922''' of the bottom semiconductor die 920''' may include a redistribution circuit as depicted in FIG. 3 and described herein. A second electrical connector 944''' extends from a bond pad 942''' on the active surface 946''' of the top semiconductor die 940''' to its corresponding terminals 968''' of the substrate 930'''.